
E 4.20 Introduction to Digital Integrated Circuit Design

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Aims and Objectives

- ◆ Understand how full-custom VLSI chips are designed
 - Different design styles and technologies
 - Design abstractions and hierarchies
 - Partitioning and architecture
- ◆ Learn to design digital IC circuits
 - Static and dynamic logic
 - Sequential logic in IC
 - Datapaths and memories
 - Testing and design-for-test
- ◆ Learn CAD tools for IC designs
 - Layout of full-custom CMOS IC's using Electric
 - Simulation using SPICE
 - Simulation using logic simulators: IRSIM & Verilog or VHDL
 - Other design verification tools
- ◆ Have fun!

Recommended Books

- ◆ Rabaey, J. et al “**Digital Integrated Circuits: A Design Perspective**” 2nd Ed. ISBN: 0131207644 (16 January, 2003) **Publisher:** Prentice Hall. (£45)
- ◆ Weste, N. H. E., and Harris, D. “**CMOS VLSI Design**” 3rd Edition, ISBN 0-321-14901-7, Addison-Wesley, 2005. (£66) – updated classic
- ◆ Smith, M.J.S. 1997. “**Application-Specific Integrated Circuits**”. Reading, MA: Addison-Wesley, 1026 p. ISBN 0-201-50022-1.
 - Good book and bargain buy (£25 - £45). Well written and worth buying.
- ◆ Glasser, L. A., and D. W. Dobberpuhl. 1985. “**The Design and Analysis of VLSI Circuits**”. Reading, MA: Addison-Wesley, 473 p. ISBN 0-201-12580-3.
 - Detailed analysis of circuits, but largely for nMOS (Hard to find).
- ◆ Mead, C. A., and L. A. Conway. 1980. “**Introduction to VLSI Systems**”. Reading, MA: Addison-Wesley, 396 p. ISBN 0-201-04358-0.
 - The first textbook in this subject, included for historical value only.

Supporting Material

- ◆ Reading material each week to support lectures
- ◆ Clearly defined targets
- ◆ Reference to textbook if relevant
- ◆ Consult my course web-page:
http://www.ee.ic.ac.uk/pcheung/teaching/ee4_asic/

Assessment, Practical work, Project

- ◆ Course work designing a chip in a group (3-4 people) - 25%
- ◆ May examination (open-book) - 75%
- ◆ Spend first 4 weeks learning CAD tools (Electric, IRSIM, SPICE)
- ◆ Spend the remain weeks working in small group to design a chip
- ◆ Deadline for completing lab work: Last day of Autumn term
- ◆ Deadline for report: Second Monday of Spring term

- ◆ Report (one per group) should include:
 - description of circuit designed (full schematic and layout)
 - block diagram showing different module in chip
 - plot of the entire chip
 - evidence that it works (from simulation plots)
 - test strategy and testbench
 - a description of contribution from each member, signed by all!

ASIC and all that! (based on slides by M. Smith)

- ◆ An **ASIC** (“a-sick”) is an **application-specific integrated circuit**
- ◆ A **gate equivalent** is a NAND gate $F = A \cdot B$, or four transistors
- ◆ History of integration:
 - **small-scale integration (SSI)**, ~10 gates per chip, 60’s)
 - **medium-scale integration (MSI)**, ~100–1000 gates per chip, 70’s)
 - **large-scale integration (LSI)**, ~1000–10,000 gates per chip, 80’s)
 - **very large-scale integration (VLSI)**, ~10,000–100,000 gates per chip, 90’s)
 - **ultra-large scale integration (ULSI)**, ~1M–10M gates per chip)
- ◆ History of technology:
 - **bipolar technology** and **transistor–transistor logic (TTL)** preceded ...
 - **metal-oxide-silicon (MOS)** technology because it was difficult to make metal-gate n-channel MOS (**nMOS** or **NMOS**)
 - the introduction of **complementary MOS (CMOS)** greatly reduced power

Topic 1

Introduction & Trends

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(Weste&Harris Ch 1; Rabaey Ch1)

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+ ASIC and all that!

- ◆ The **feature size** is the smallest shape you can make on a chip and is measured in λ or **lambda**
- ◆ Origin of ASICs:
 - **standard parts** - initially used to design **microelectronic systems**
 - gradually replaced with a combination of **glue logic**, **custom ICs**, **dynamic random-access memory (DRAM)** and **static RAM (SRAM)**
- ◆ Key conferences: The IEEE Custom Integrated Circuits Conference (CICC) and IEEE International ASIC Conference document the development of ASICs
- ◆ **Application-specific standard products (ASSPs)** are a cross between standard parts and ASICs

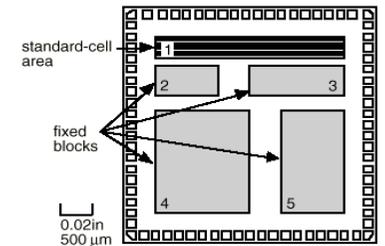
Full-custom ASIC

- ◆ All mask layers are customized in a **full-custom ASIC**.
- ◆ It only makes sense to design a full-custom IC if there are no libraries available.
- ◆ Full-custom offers the highest performance and lowest part cost (smallest die size) with the disadvantages of increased design time, complexity, design expense, and highest risk.
- ◆ Microprocessors were exclusively full-custom, but designers are increasingly turning to semicustom ASIC techniques in this area too.
- ◆ Other examples of full-custom ICs or ASICs are requirements for high-voltage (automobile), analog/digital (communications), or sensors and actuators.

Standard-Cell-Based ASICs

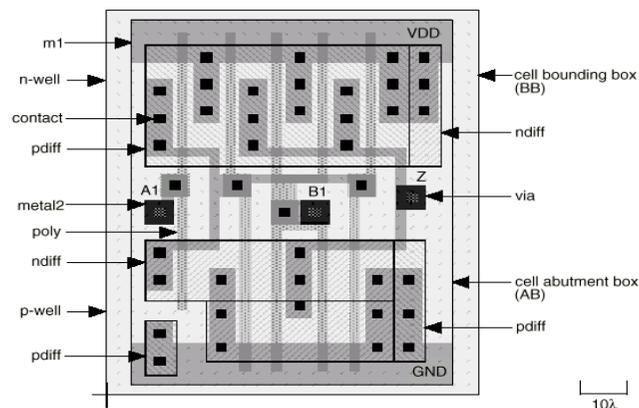
A cell-based ASIC (CBIC—"sea-bick")

- Standard cells
- Possibly **megacells**, **megafunctions**, **full-custom blocks**, **system-level macros (SLMs)**, **fixed blocks**, **cores**, or **Functional Standard Blocks (FSBs)**
- All mask layers are customized—transistors and interconnect
- Custom blocks can be embedded
- Manufacturing lead time is about eight weeks.



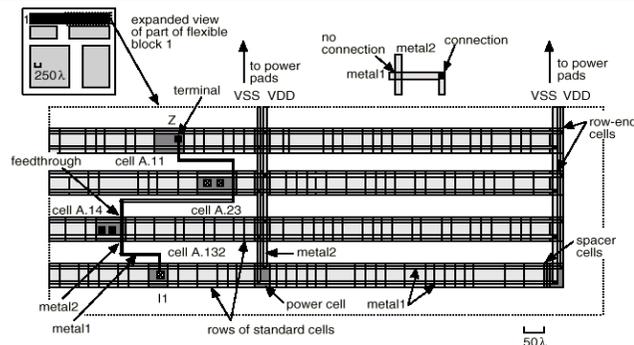
- ◆ In **datapath (DP)** logic we may use a **datapath compiler** and a **datapath library**. Cells such as **arithmetic and logical units (ALUs)** are **pitch-matched** to each other to improve timing and density.

Full-custom Standard Cell



Looking down on the layout of a **standard cell** from a **standard-cell library**

Cell-based IC



- ◆ Routing a CBIC (cell-based IC)
 - A "wall" of standard cells forms a **flexible block**
 - **metal2** may be used in a **feedthrough cell** to cross over cell rows that use **metal1** for wiring
 - Other wiring cells: **spacer cells**, **row-end cells**, and **power cells**

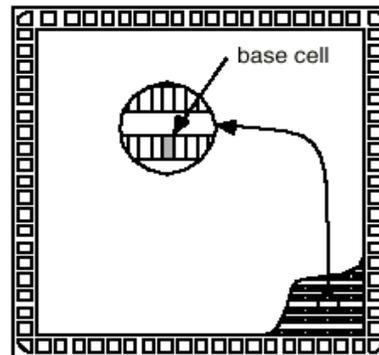
Gate-Array-Based ASICs

- ◆ A **gate array, masked gate array, MGA, or prediffused array** uses **macros (books)** to reduce **turnaround time** and comprises a **base array** made from a **base cell** or **primitive cell**. There are three types:

- Channeled gate arrays
- Channelless gate arrays
- Structured gate arrays

- ◆ A **channeled gate array**

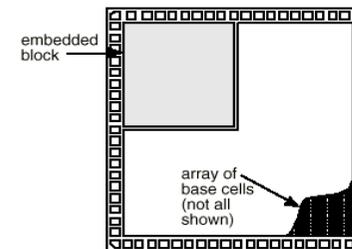
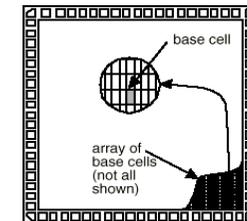
- Only the interconnect is customized
- The interconnect uses predefined spaces between rows of base cells
- Manufacturing lead time is between two days and two weeks



Gate-Array-Based ASICs (con't)

- ◆ A **channelless gate array (channel-free gate array, sea-of-gates array, or SOG array)**

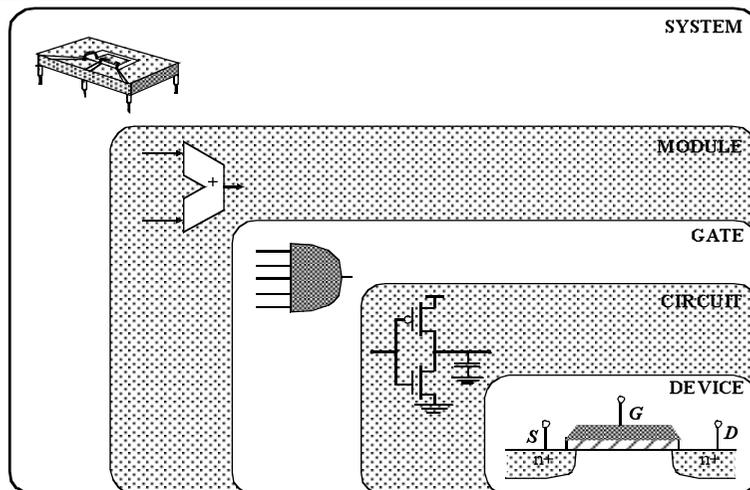
- Only some (the top few) mask layers are customized — the interconnect
- Manufacturing lead time is between two days and two weeks.



- ◆ An **embedded gate array or structured gate array (masterslice or masterimage)**

- Only the interconnect is customized
- Custom blocks (the same for each design) can be embedded
- Manufacturing lead time is between two days and two weeks.

Design Abstraction Levels

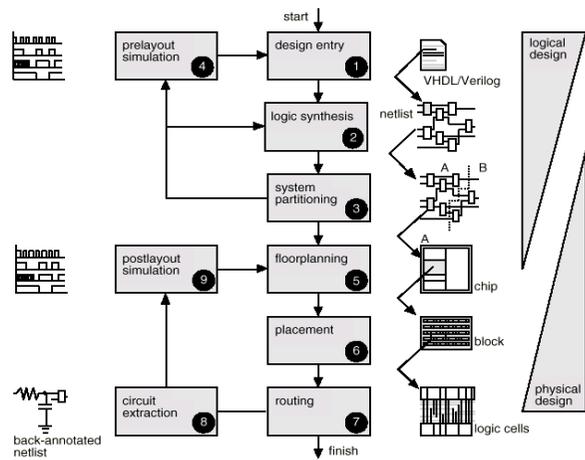


Design Flow

A **design flow** is a sequence of steps to design an ASIC

- ◆ **Design entry.** Using a **hardware description language (HDL)** or schematic entry.
- ◆ **Logic synthesis.** Produces a **netlist**—logic cells and their connections.
- ◆ **System partitioning.** Divide a large system into ASIC-sized pieces.
- ◆ **Pre-layout simulation.** Check to see if the design functions correctly.
- ◆ **Floorplanning.** Arrange the blocks of the netlist on the chip.
- ◆ **Placement.** Decide the locations of cells in a block.
- ◆ **Routing.** Make the connections between cells and blocks.
- ◆ **Extraction.** Determine the resistance and capacitance of the interconnect.
- ◆ **Postlayout simulation.** Check to see the design still works with the added loads of the interconnect.

Design Flow (con't)

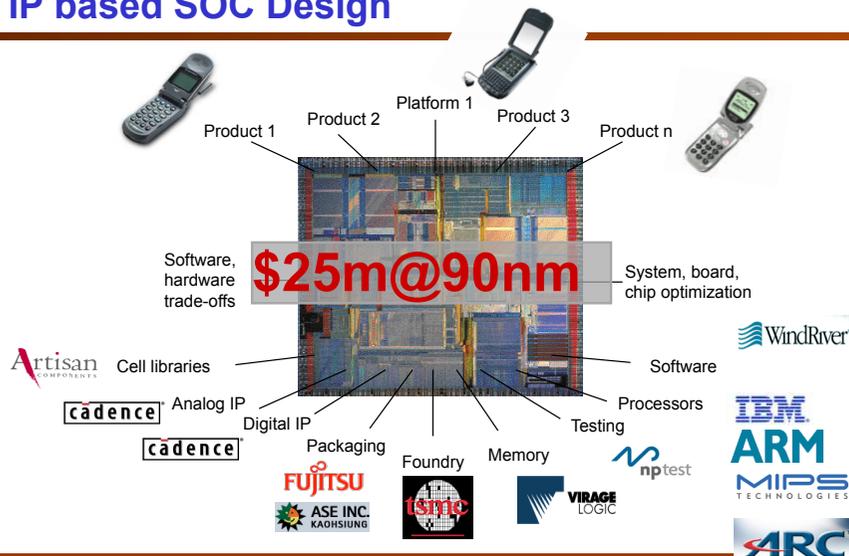


ASIC design flow. Steps 1–4 are **logical design**, and steps 5–9 are **physical design**

ASIC Cell Libraries

- ◆ Use a **design kit** from the **ASIC vendor**
 - Usually a **phantom library**—the cells are empty boxes, or **phantoms**, you **hand off** your design to the ASIC vendor and they perform **phantom instantiation** (Synopsys CBA)
- ◆ Buy an **ASIC-vendor library** from a **library vendor**
 - **buy-or-build decision**. You need a **qualified cell library** (qualified by the **ASIC foundry**) If you own the masks (the **tooling**) you have a **customer-owned tooling solution** (which is becoming very popular)
- ◆ Build your own cell library
 - involves a complex **library development process**: **cell layout** ; **behavioral model** ; Verilog/VHDL model ; **timing model** ; test strategy ; **characterization** ; **circuit extraction** ; **process control monitors (PCMs)** or **drop-ins** ; **cell schematic** ; cell icon ; **layout versus schematic (LVS)** check; **cell icon** ; **logic synthesis** ; **retargeting** ; **wire-load model** ; **routing model**; **phantom**

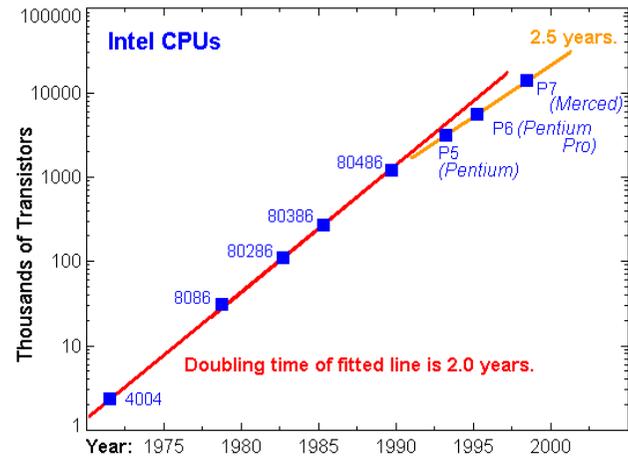
IP based SOC Design



Challenges in VLSI

- ◆ Gordon Moore, co-founder of Intel, observed in 1965 that number of transistors per square inch in ICs doubled every year.
- ◆ In subsequent years, the pace slowed down a bit, but density has **doubled approximately every 18 months**, and this is the current definition of Moore's Law.
- ◆ Most experts, including Moore himself, expect Moore's Law to hold for at least another two decades.

+ Moore's Law

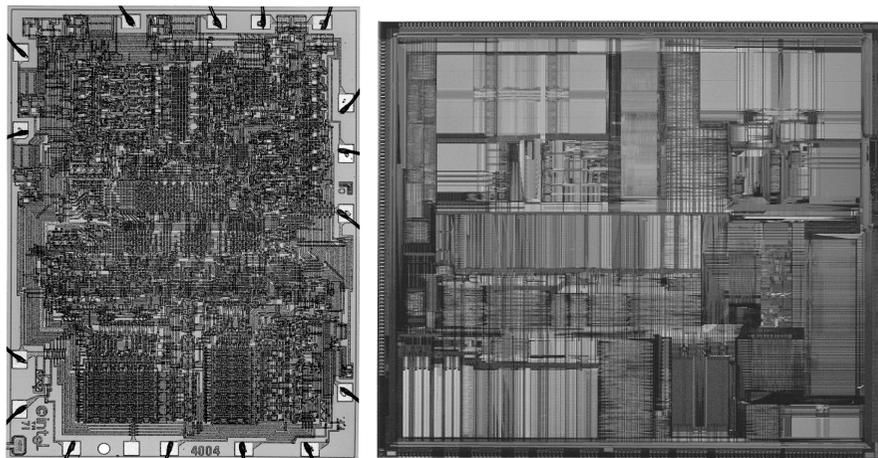


Source: Intel

Intel microprocessors

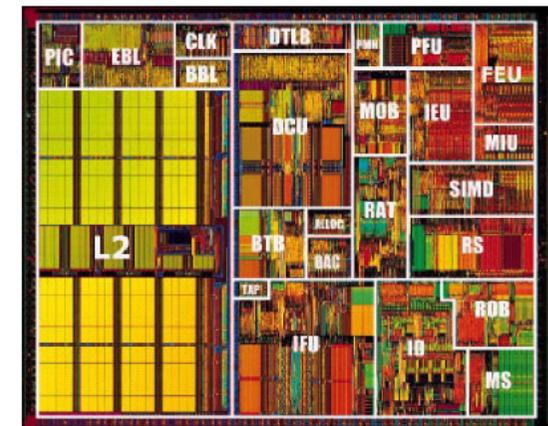
	Year of introduction	Transistors
4004	1971	2,250
8008	1972	2,500
8080	1974	5,000
8086	1978	29,000
286	1982	120,000
386™ processor	1985	275,000
486™ DX processor	1989	1,180,000
Pentium® processor	1993	3,100,000
Pentium II processor	1997	7,500,000
Pentium III processor	1999	24,000,000
Pentium 4 processor	2000	42,000,000

Intel Microprocessor - 4004 & Pentium II

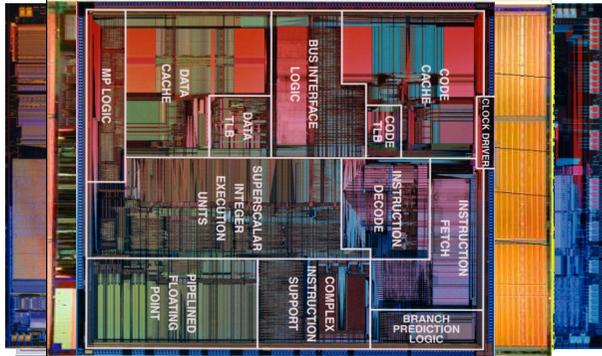


Intel Pentium III

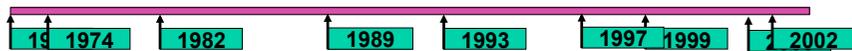
- ◆ Intel Pentium III
- ◆ 0.18 micron process
- ◆ 28 million transistors



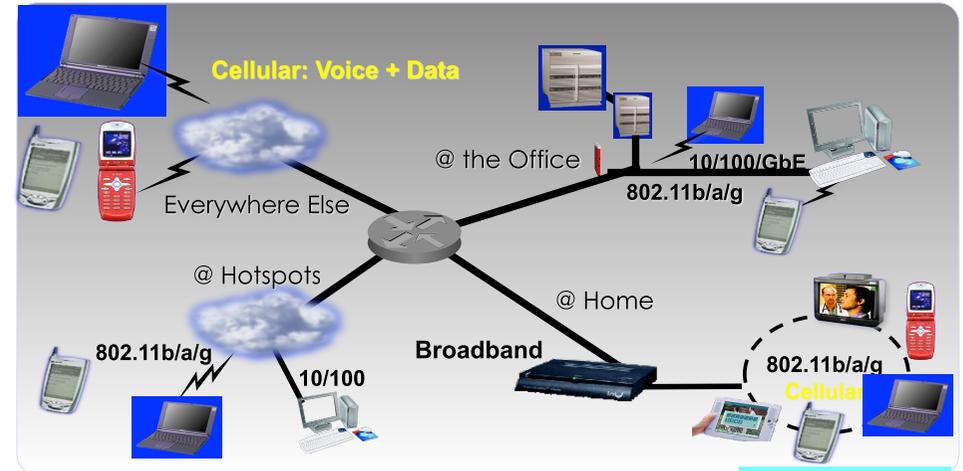
The Complexity Problem



Intel Pentium IV
Transistors: 291,000,000



Any Device, Any Time, Anywhere

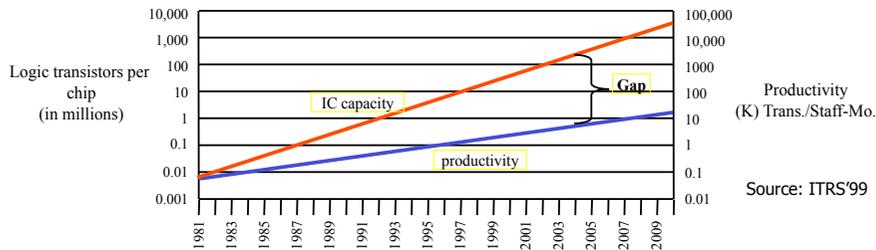


Source: Greg Spirakis

2010: 1.5 billion interconnected PCs,
2.5 billion interconnected PDAs

Very Few Companies Can Design High-End ICs

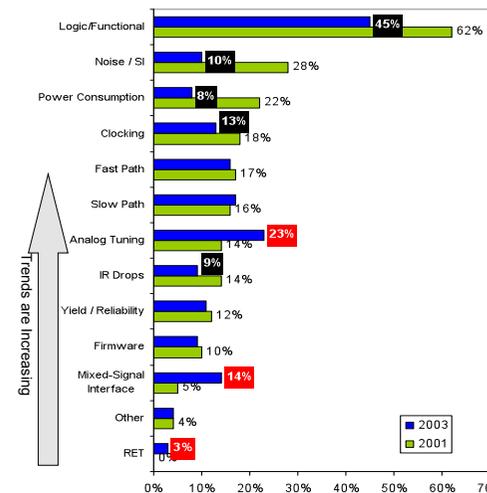
Design productivity gap



Source: ITRS'99

- ◆ Designer productivity growing at slower rate
 - 1981: 100 designer months → ~\$1M
 - 2002: 30,000 designer months → ~\$300M

Less First Silicon Success and the Changing Rate of Failures

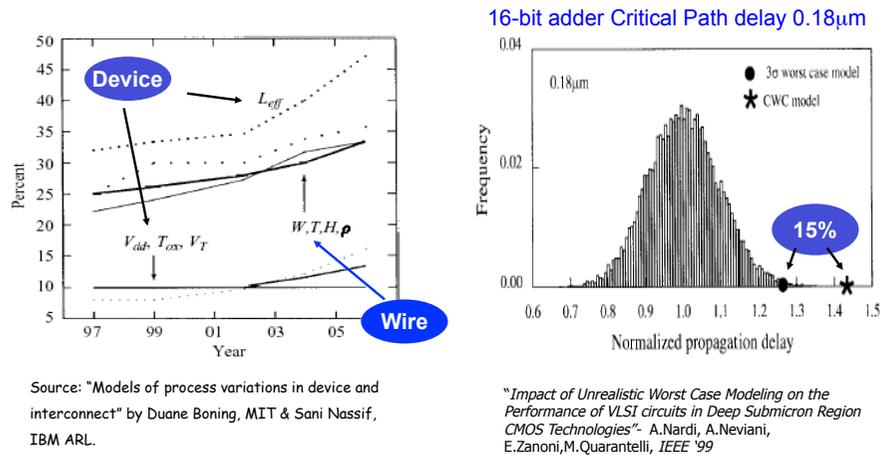


◆ First silicon success rates declining

- **First Silicon OK**
48% in 2000
39% in 2002
34% in 2003
- **Third Silicon OK**
>90% in 2000
>70% in 2002
>60% in 2003

Collett International Research: 2000, 2002 Functional Verification Studies; 2003 Design Closure Study, 01/04

Process Variability Dealing with Uncertainty



Silicon in 2009

Die Area: 2.5x2.5 cm
Voltage: 0.6 V
Technology: 0.07 μ m

	Density (Gbits/cm ²)	Access Time (ns)
DRAM	8.5	10
DRAM (Logic)	2.5	10
SRAM (Cache)	0.3	1.5

	Density (Mgates/cm ²)	Max. Ave. Power (W/cm ²)	Clock Rate (GHz)
Custom	25	54	3
Std. Cell	10	27	1.5
Gate Array	5	18	1
Single-Mask GA	2.5	12.5	0.7
FPGA	0.4	4.5	0.25

Further Reading

- ◆ Moore's Law article
- ◆ International Technology Roadmap for Semiconductors (2009 Edition)

<http://www.itrs.net/Links/2009ITRS/Home2009.htm>

Assignment 1

- ◆ Objective: For you to be familiar with the factors that drives the future of integrated circuit technology
- ◆ Specification: You are required to read:

2009_Design.pdf (The ITRS Chapter on Design)

- ◆ Deliverables: You are required to prepare a PowerPoint presentation (say for a 5 minutes talk with around 5-6 slides) to explain a part of the document you find most interesting to your fellow engineers.
- ◆ Deadline: You must complete this by Monday 25 October 2010. You have to submit your slides through BlackBoard. (This is a "tick-box" exercise that you must complete, but will not contribute to your final marks.)